ABSTRACT OF THE DISCLOSURE

The invention encompasses stacked semiconductor devices including gate stacks, wordlines, PROMs, conductive interconnecting lines, and methods for forming such structures. In one aspect, the invention includes a method of forming a conductive line comprising: a) forming a polysilicon layer; forming a silicide layer against the polysilicon layer; b) providing a conductivity-enhancing impurity within the silicide layer; and c) providing the polysilicon layer and the silicide layer into a conductive line shape. In another aspect, the invention includes a programmable-read-only-memory device comprising: a) a first dielectric layer over a substrate; b) a floating gate over the first dielectric layer; c) a second dielectric layer over the floating gate; d) a conductive line over the second dielectric layer; and e) a metal-silicide layer over the conductive line, the metal-silicide layer comprising a Group III dopant or a Group V dopant.